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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,492	02/05/2002	Michael J. Tsecouras	TI-33116	7292
23494	7590	08/13/2004	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			LE, DUY K	
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		2685		
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Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/068,492	TSECOURAS, MICHAEL J.
	Examiner	Art Unit
	Duy K Le	2685

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on \_\_\_\_\_.  
 2a) This action is **FINAL**.      2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-29 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_ is/are allowed.  
 6) Claim(s) 1-29 is/are rejected.  
 7) Claim(s) \_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____. 
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____. 	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-5, 11-15, 18-21, 24-25, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,341,402 to Matsushita et al. in view of Orndorff (U.S. Patent 5,640,697).

As to claim 1, Figure 7 in Matsushita shows a digital amplifier adaptive pulse frame rate frequency control system comprising:

a sample rate converter (74) (see Col. 6, lines 40-43);

a programmable controller (75) operational to generate control data bits (see Col. 6, lines 43-59); and

a system clock generator (76) operational to generate a sample rate converter master clock signal in response to the control data bits such that the sample rate converter generates output data at a sample rate determined by the control data bits (see Col. 6, lines 43-48).

However, the Matsushita reference does not disclose a programmable controller operational in response to user selected input frequency data to generate control data bits. The Orndorff reference teaches a programmable controller operational in response to user selected input frequency data to generate control data bits (see Figure 3, Col. 3, lines 9-15, Col. 5, lines 9-28, Col. 8, lines 12-16, and Col. 11, line 59 to Col. 12 line 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Matsushita to comprise a programmable controller operational in response to user selected input frequency data to generate control data bits, as taught by Orndorff, in order to program the controller to respond to inputs for tuning.

As to claims 2, 13, and 19, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 1, 12, and 18 wherein the programmable controller comprises a data processing device selected from the group consisting of a computer, a digital signal processor (DSP), a CPU, and a micro-controller (Matsushita: see Figure 6, and Col. 5, line 62 to Col. 6, line 18. Orndorff: see Col. 5, lines 9-16).

As to claims 3, 14, and 20, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 1, 12, and 18 wherein the system clock generator comprises a frequency controller selected from the group consisting of a digital frequency synthesizer, and a programmable phase-locked loop (Matsushita: see Col. 5, lines 10-27).

As to claims 4, 15, and 21, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 1, 12, and 18 wherein the system clock generator is further operational to generate audio clock signals at the sample rate determined by the control data bits (Matsushita: see Col. 6, lines 43-48 and Figure 7. It is inherent that if the received signal is audio clock signal, then the system clock generator generates audio clock signals at the determined sample rate).

As to claims 5 and 24, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 4 and 18 wherein the system clock

generator is further operational to generate sample clock signals at the sample rate determined by the control data bits (Matsushita; see Col. 6, lines 43-48 and Figure 7).

As to claim 11, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claim 1 wherein the sample rate converter comprises a digital asynchronous sample rate converter (Matsushita; “A/D converter 74” in Figure 7 and Col. 6, lines 40-43).

As to claim 12, Figure 7 in Matsushita shows a digital amplifier adaptive pulse frame rate frequency control system comprising:

a digital asynchronous sample rate converter (74) operational to generate output audio data in response to input audio data, an input audio clock and a master clock (see Col. 6, lines 40-43);

a programmable controller (75) operational to generate control data bits (see Col. 6, lines 43-59);

a decoder operational to decode the control data bits (see Col. 6, lines 43-59. It is inherent that there is a decoder in the sampling clock generator 76 to decode the control data from the microprocessor 75); and

a system clock generator (76) operational to generate the master clock in response to the decoded control data bits such that the digital asynchronous sample rate converter generates the output data at a sample rate determined by the user selected input frequency information (see Col. 6, lines 43-48).

However, the Matsushita reference does not disclose a programmable controller operational in response to user selected input frequency information to generate control data bits,

wherein the input frequency information is selected from the group consisting of wireless, cellular telephone, Bluetooth, RF, IF, LCO, AM, FM, and TV band frequencies. The Orndorff reference teaches a programmable controller operational in response to user selected input frequency information to generate control data bits, wherein the input frequency information is selected from the group consisting of wireless, cellular telephone, Bluetooth, RF, IF, LCO, AM, FM, and TV band frequencies (see Figure 3, Col. 1, lines 13-20, Col. 3, lines 9-15 and 23-30, Col. 4, lines 37-42, Col. 5, lines 9-28, Col. 5, line 44 to Col. 8, line 20, and Col. 11, line 59 to Col. 12 line 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Matsushita to comprise a programmable controller operational in response to user selected input frequency information to generate control data bits, wherein the input frequency information is selected from the group consisting of wireless, cellular telephone, Bluetooth, RF, IF, LCO, AM, FM, and TV band frequencies, as taught by Orndorff, in order to program the controller to respond to inputs for tuning.

As to claim 18, what is cited in claim 12 is applicable to this claim 18. Claim 18 is the same as claim 12, except “means” is used in place of an element (e.g., programmable controlling means in claim 18 versus a programmable controller in claim 12).

As to claim 25, Figure 7 in Matsushita shows a method of controlling the pulse-frame rates for a digital amplifier output signal comprising the steps of:

providing a pulse-frame rate frequency control system having a programmable controller (75), a system clock generator (76), and a digital asynchronous sample rate converter (74)

operational to generate output audio data at a first sample rate in response to input audio data and further in response to input audio clocks (see Col. 6, lines 40-59);

communicating the control data bits to the system clock such that the system clock generates a master clock for the digital asynchronous sample rate converter at a new sample rate and further such that the system clock generates output audio clocks at the new sample rate (see Col. 6, lines 43-59); and

adapting the digital asynchronous sample rate converter output audio data at a first sample rate to conform to the new sample rate determined by the master clock (see Col. 6, lines 40-43).

However, it does not disclose communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data. The Orndorff reference teaches communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data (see Figure 3, Col. 3, lines 9-15, Col. 5, lines 9-28, Col. 8, lines 12-16, and Col. 11, line 59 to Col. 12 line 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Matsushita to comprise the step of communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data, as taught by Orndorff, in order to program the controller to respond to inputs for tuning.

As to claim 28, Matsushita-Orndorff discloses the method of claim 25 wherein the step of communicating user selected input frequency data to the controller such that the controller

generates control data bits determined by the user selected input frequency data comprises the step of providing a look-up table of pulse-frame frequencies (output digital asynchronous sample rate converter clock generator frequencies) versus station data selected from the group consisting of RF, IF, LCO, AM, FM, TV station, wireless, cellular telephone and Bluetooth frequencies, that can be accessed by the controller to determine the control data bits (Orndorff: see Figure 3, Col. 1, lines 13-20, Col. 3, lines 9-15 and 23-30, Col. 4, lines 37-42, Col. 5, lines 9-28, Col. 5, line 44 to Col. 8, line 20, and Col. 11, line 59 to Col. 12 line 8).

As to claim 29, Matsushita-Orndorff discloses the method of claim 25 wherein the step of communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data comprises the step of providing an algorithm to select pulse-frame frequencies (output digital asynchronous sample rate converter clock generator frequencies) versus station data selected from the group consisting of RF, IF, LCO, AM, FM, TV station, wireless, cellular telephone and Bluetooth frequencies, that can be accessed by the controller to determine the control data bits (Orndorff: see Figure 3, Col. 1, lines 13-20, Col. 3, lines 9-15 and 23-30, Col. 4, lines 37-42, Col. 5, lines 9-28, Col. 5, line 44 to Col. 8, line 20, and Col. 11, line 59 to Col. 12 line 8).

3. Claims 6-10, 16-17, 22-23, and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,341,402 to Matsushita et al. in view of Orndorff (U.S. Patent 5,640,697) and further in view of Midya et al. (U.S. Patent Application Publication 2002/0180518 A1).

As to claims 6, 16, and 22, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 4, 15, and 21. However, it does

not disclose a digital amplifier responsive to the system clock generator audio clock signals and the sample rate converter output data such that the digital amplifier output switches at a pulse-frame rate determined by the system clock generator audio clock signals and the sample rate converter output data. The Midya reference teaches a digital amplifier responsive to the system clock generator audio clock signals and the sample rate converter output data such that the digital amplifier output switches at a pulse-frame rate determined by the system clock generator audio clock signals and the sample rate converter output data (see Figure 1 and page 1, col. 2, paragraphs [0010] – [0011]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Matsushita-Orndorff to further comprise a digital amplifier responsive to the system clock generator audio clock signals and the sample rate converter output data such that the digital amplifier output switches at a pulse-frame rate determined by the system clock generator audio clock signals and the sample rate converter output data, as taught by Midya, in order to provide error correction in digital amplifiers.

As to claims 7, 17, and 23, Matsushita-Orndorff-Midya discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 6, 16, and 22 wherein the digital amplifier output further switches at a pulse-frame rate to minimize interference associated with keep-out bands for frequencies related to a desired source (Midya: see page 2, col. 1, paragraph [0012]).

As to claim 8, Matsushita-Orndorff-Midya discloses the digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are

associated with frequencies selected from the group consisting of AM, FM and TV band frequencies (Orndorff: see Col. 1, lines 13-15, Col. 3, lines 23-30 and Col. 4, lines 37-42).

As to claim 9, Matsushita-Orndorff-Midya discloses the digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are associated with frequencies selected from the group consisting of radio frequency (RF), intermediate frequency (IF), and Local Control Oscillator (LCO) frequencies (Orndorff: see Col. 5, line 44 to Col. 8, line 20).

As to claim 10, Matsushita-Orndorff-Midya discloses the digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are associated with wireless communication frequencies selected from the group consisting of cellular telephone frequencies and Bluetooth frequencies (Matsushita: see Col. 1, lines 7-10 and Col. 5, lines 42-45. Orndorff: see Col. 1, lines 13-20 and Col. 13, line 28 to Col. 14, line 4).

As to claim 26, Matsushita-Orndorff discloses the method according to claim 25. However, it does not disclose the steps of: providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate. The Midya reference teaches the steps of: providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate (see Figure 1 and page 1, col. 2, paragraphs [0010] –

[0011]); and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate (see Figure 1 and page 1, col. 2, paragraphs [0010] – [0011]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Matsushita-Orndorff to comprise the steps of: providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate, as taught by Midya, in order to provide error correction in digital amplifiers.

As to claim 27, Matsushita-Orndorff discloses the method according to claim 25 with keep-out bands associated with the frequency group consisting of AM, FM, and TV band frequencies ((Orndorff: see Col. 1, lines 13-15, Col. 3, lines 23-30 and Col. 4, lines 37-42). However, it does not disclose the steps of: providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate that substantially

minimizes interference minimizes interference with keep-out bands. The Midya reference teaches the steps of: providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate (see Figure 1 and page 1, col. 2, paragraphs [0010] – [0011]); and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate that substantially minimizes interference minimizes interference with keep-out bands (see Figure 1 and page 1, col. 2, paragraphs [0010] – [0011]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Matsushita-Orndorff to comprise the steps of: providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate that substantially minimizes interference minimizes interference with keep-out bands, as taught by Midya, in order to provide error correction in digital amplifiers.

### ***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

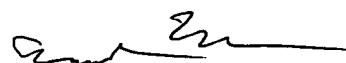
- a. Hotto (U.S. Patent 6,236,845) discloses system and method for radio signal reconstruction using signal processor.
- b. Sakurai (U.S. Patent 4,531,232) discloses radio receiver apparatus for vehicle.
- c. Rasor (U.S. Patent 5,848,355) discloses frequency synthesizer correction using a temperature responsive divisor control.
- d. Vitallo et al. (U.S. Patent Application Publication 2002/0160816 A1) discloses apparatus and method for receiving television audio signals in a mobile vehicle.
- e. Skerlos (U.S. Patent 4,317,227) discloses multi-mode automatic channel frequency synthesis system.
- f. Robin (U.S. Patent 5,745,848) discloses method and apparatus for eliminating interference caused by spurious signals in a communication device.
- g. Dang et al. (U.S. Patent 5,949,472) discloses method and apparatus for tuning channels for CATV and television applications.
- h. Belisomi (U.S. Patent 4,373,208) discloses circuit arrangement for tuning into one of a number of radioelectric signals.
- i. Nagata (U.S. Patent 5,390,344) discloses FM audio signal receiver having a characteristic control function.
- j. Goeddel et al. (U.S. Patent 6,665,356) discloses sample timing control for demodulation of phase-modulated signals.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duy K Le whose telephone number is 703-305-5660. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F Urban can be reached on 703-305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Duy Le  
August 3, 2004



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